

Scanworks Boundary Scan Test

- Test of PCB can be performed from as few as 4 pins on a connector.
- Test coverage is dependant upon JTAG to JTAG signaling.
- Shorts, Opens, JTAG Chain and Interconnect testing.
- Interface logic testable if controlled by JTAG or IO Pod signals.
- Memory devices testable if controlled by JTAG or IO Pod signals.
- Programming of flash devices controlled by JTAG or IO Pod signals.
- ISP for FPGA, CPLD.
- Execution of User Code and BIST.
- GUI based software development system.
- Interactive debugging.
- DFT analysis available.
- Online component libraries for JTAG, logic, memory & flash.
- Test Fixture may be necessary to access power or control signals.